Insulating Biomaterials
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By the:

Biomedical Microelectronics Laboratory
Biomedical Engineering Center, Massachusetts Institute of Technology
West Roxbury VA Medical Center

Contributors:
David J. Edell, PI
Karen K. Gleason, Chemical Engineering
Bruce C. Larson, Grad Student, Electrical Engineering
Hilton Lewis, Grad Student, Chemical Engineering
Sean Sexton, Electronics

Introduction

This report focuses on long term saline soak testing of Kapton/Polyimide structures from Troy Nagle's lab at North Carolina State University and on the performance of recently received CMOS integrated circuit test devices for monitoring circuit elements during long term saline soak and animal implantation.

Kapton/Polyimide Structures

Troy Nagle's lab at North Carolina State University prepared five different Kapton based interdigitated electrode arrays to test various approaches to preparation of implantable Kapton based structures. All structures were formed by deposition of gold traces on Kapton substrates followed by coating with an insulator. The insulators used were Dow Corning silicone T-RTV, Dupont Polyimide 2721, Dupont Polyimide 2723, Dupont PC1025, and Dupont Dow3-1753. Initially, samples were dry tested for 3 weeks before the addition of saline to establish a baseline of bulk resistivity. Following addition of saline, many samples survived for an additional 2 weeks. The Dupont Polyimide 2721 coated samples were the most reliable thus far, with all four devices surviving saline soak for over 6 months thus far.

The graphs shown in Figure 1 were constructed using measured data from test structures and results of the simple model shown in Figure 2. The test structures were interdigitated electrode arrays on Kapton substrates with Dupont 2721 Polyimide overcoating the electrodes. They were provided by Troy Nagle's lab at North Carolina State University (NCSU).

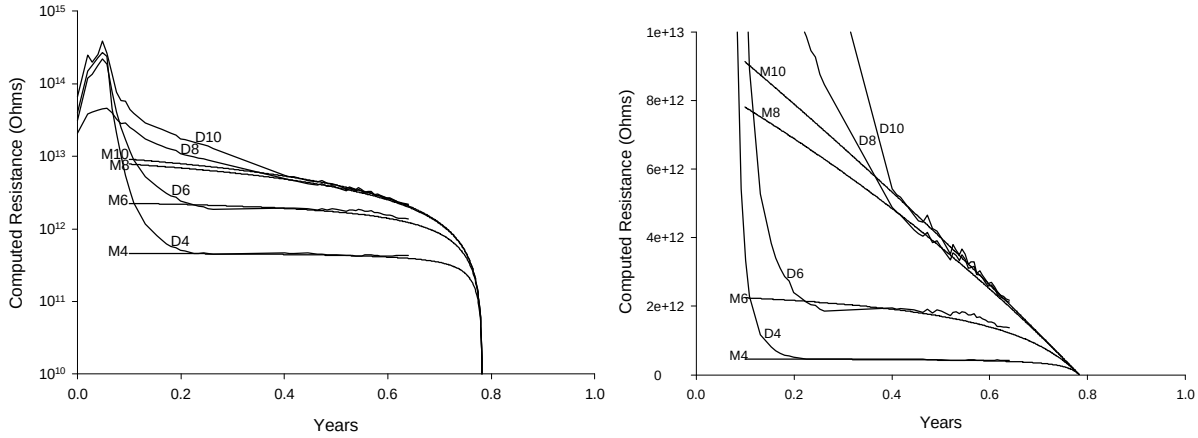
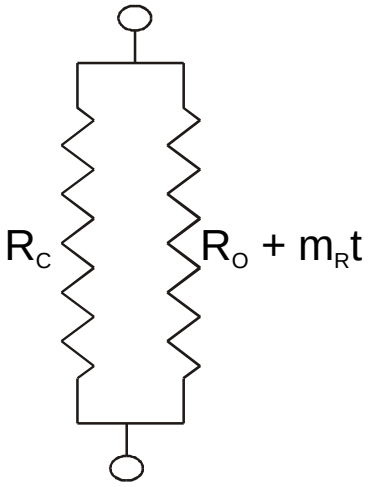


Figure 1: Data (D) from Kapton/Polyimide mini-ribbon cable process from NCSU interdigitated electrode arrays shown on log and linear scales together with data from simple parallel resistance model (M).

The model used to extrapolate the decay in performance is shown in Figure 2. The model consisted of a constant resistance (R_C) in parallel with a second resistance that was time dependent. This time dependent resistance was modeled using an equation found by performing a linear regression on the most recent three months of data. The recent data was used because the effects of the initial transients caused by hydration

had settled out for the most part. Also, it was where we would expect the contribution from the parallel constant resistances to be as low as possible.



$$R(t) = \frac{1}{\frac{1}{R_C} + \frac{1}{R_O + m_R t}}$$

Figure 2: Simple model for observed data from Kapton soaks consisting of a constant resistance in parallel with time dependent resistor.

For the lower resistivity devices, the constant resistance term was estimated from the middle segment of the data which was fairly constant over time for the devices that exhibited the highest leakage initially. Because there was no clear region where the resistance didn't change for Electrometer 8 and 10 devices, the constant resistance term in the model was adjusted to provide an adequate fit to the data at the 0.5 year mark where the last linear data segment joined the middle, flat segments.

The resulting model data fit the last segment of the real data well as it should. It may be that if there truly is a degradation process that begins as a high resistance and falls over time as evidenced by the high resistance devices, there will be an apparently sudden demise of the low resistance devices at about 0.77 years. The apparent rapid demise of the devices after about 0.7 years is actually due to the increasing dominance of the time dependent resistance term as the it becomes equal to (cuts total resistance in half) and then lower than the constant term. In fact, from prior work on wire samples coated with polyimide, there is a relatively sudden failure mode at about 8 months following saline immersion. While it is unlikely that this model will adequately predict the exact data to come as the soaking continues, it does provide some insight.

This example illustrates a subtle problem with lifetime testing and estimation. There is no way to determine if one parameter is masking a second process until the second process progresses far enough to be observable. That is, if all of the devices had the same low value constant resistance that Electrometer 4 exhibited, there would have been no way to tell that the second process was occurring. Thus, until the second process becomes visible, any predictions based on the data would grossly overestimate the lifetime of the device.

Constant awareness of the potential for masking of degradation processes can help minimize the risk of having implantable devices fail "out of the blue" because an unrecognized process had not been elicited during testing.

Integrated Circuit Test Chips

The CMOS integrated circuits were received at the end of December were evaluated this quarter. While the circuits were functional, their dynamic range was limited by a design flaw in the integrator reset circuitry. New circuits were designed and submitted for fabrication based on the performance and modeling of the previous design.

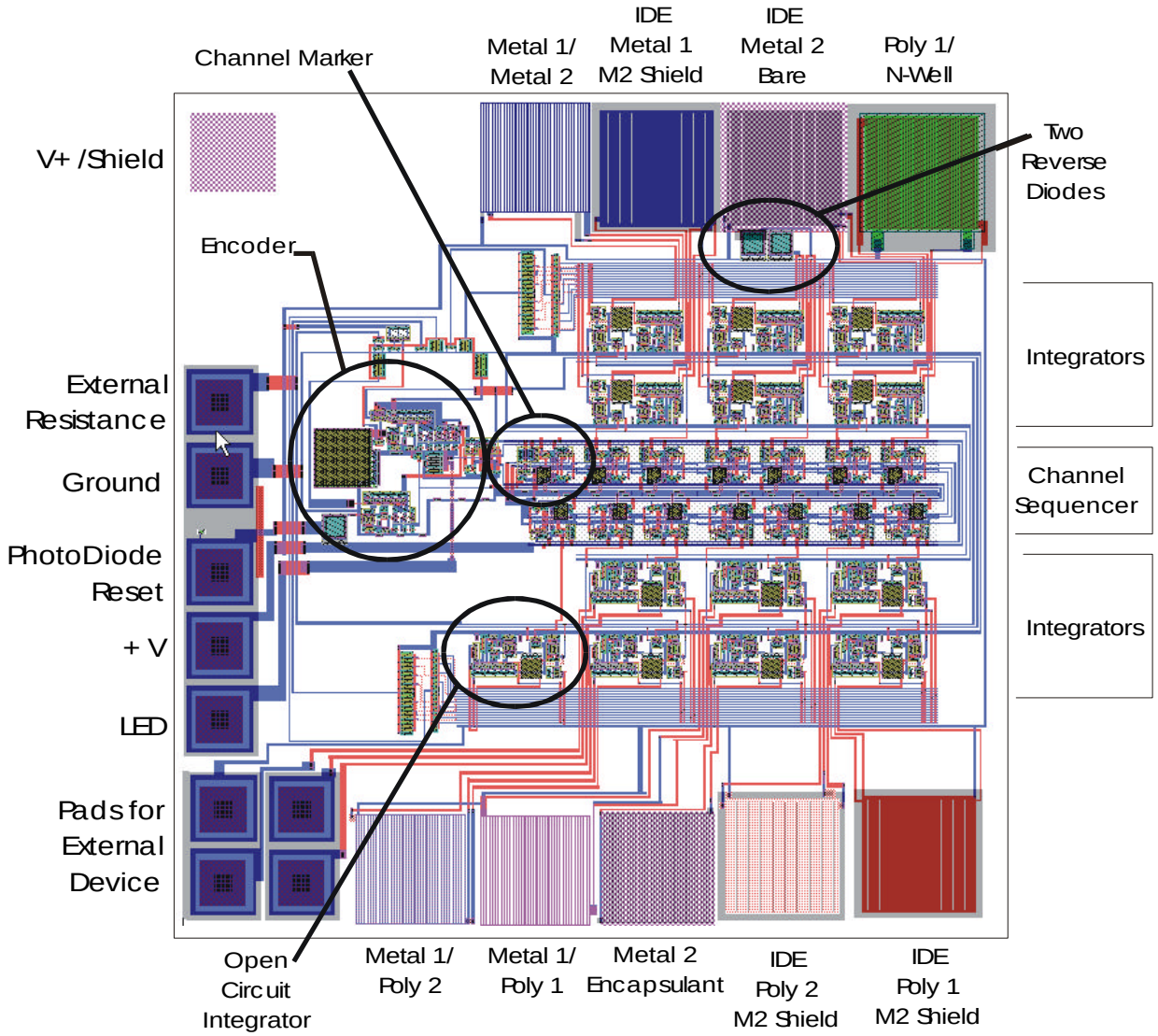


Figure 3: PassChip overview showing pad arrangement, test devices around periphery, channel sequencer and encoder in center corridor, and integrators between sequencer and test devices.

An early circuit design is shown in Figure 3. There were 5 circuit related bond pads for connecting an external bias setting resistor, power supply, the LED output, and the photodiode reset for initializing the shift register after power up. There is an on-chip

photodiode for the same purpose. The entire circuit except for the reset photodiode is shielded by Metal 2.

Pads for an external device were included to allow attachment of wire loops or some other external test device. They could also be connected with short wire loops to test bond pad leakage currents directly. The central corridor of the chip contains a loop of low power shift registers that continually cycle through the integrators to function as a channel sequencer. Double rows of integrators are located on either side of the shift registers. The test devices are connected to the integrators. The outputs of the integrators are bussed to the readout stage. The readout stage consists of switching to allow resetting of the readout capacitor high, then setting of the capacitor to the integrator output voltage using a p-channel source follower on the output of the integrator being addressed. A 10nA current source pulls off the charge from the readout capacitor and then resets the readout capacitor. During the reset sequence, a pulse is generated for the LED transmitter.

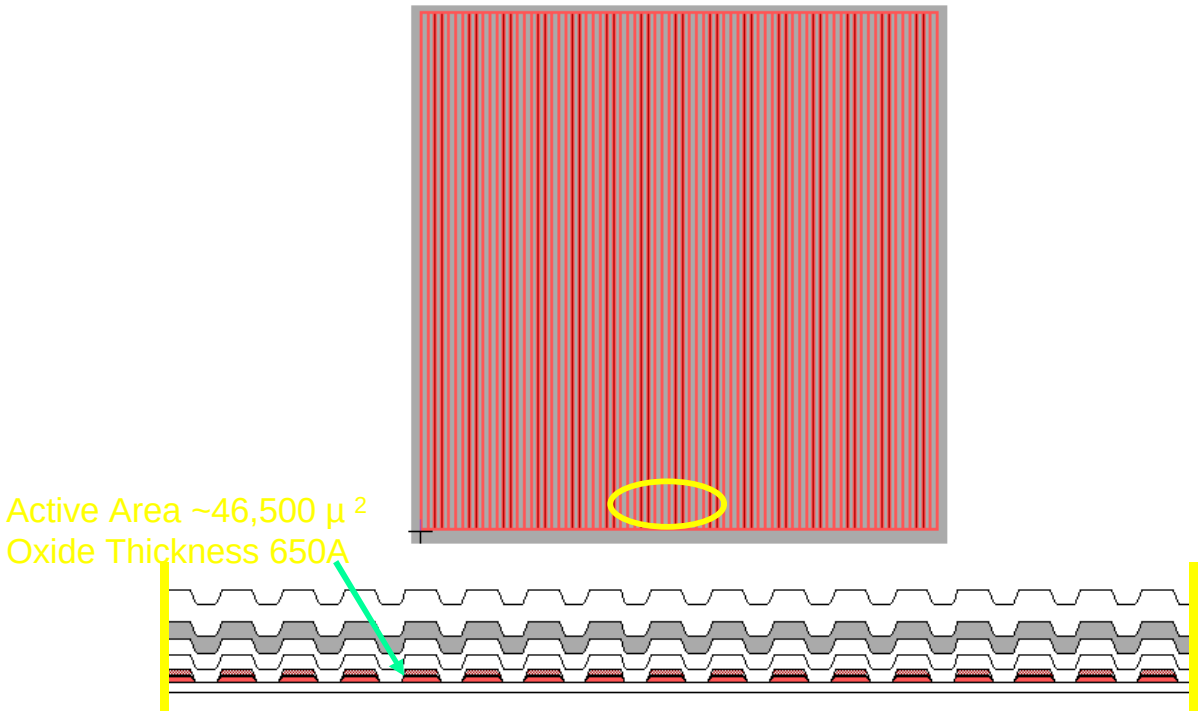


Figure 4: Example of vertical test structure shielded by Metal 2 (solid grey squiggle). Arrow points to one line of this multi-line structure with polysilicon 1 and polysilicon 2 separated by a thin silicon dioxide layer.

There were 14 channels included on this implementation. One channel was used for identifying Channel 1. Another channel was used to measure the open circuit leakage current of an integrator stage. Two channels were used to monitor the reverse biased leakage current of 3600µm^2 diodes. One of the diodes was shielded with Metal 2 and the other was not. Another channel was used for monitoring the external device bond pads. The remaining 9 devices were used for on-chip test structures. The on-chip test structures were of 2 varieties. One was an array of conductive fingers overlaying a

second array of conductive fingers with the dielectric to be tested in between. These can be thought of as vertical testers and are designed to detect failure of the dielectric between two layers. An example of a vertical tester is shown in Figure 4. This structure consists of an array of lines of polysilicon on 2 layers separated by a thin silicon dioxide dielectric. The integrator will acquire electrons that flow from one polysilicon layer to the other through the thin dielectric. The active area is large and there are 2μm wide slots between every finger thereby ensuring that the device will be sensitive to water and ionic contamination. Vertical test devices included Metal 1 – Metal 2, Polysilicon 1 – N-Well, Metal 1 – Polysilicon 1, and Metal 1 to Polysilicon 2, and Metal 2 –Encapsulant. The Metal 2 – Encapsulant device was to measure the bulk resistivity of whatever encapsulant was used to protect the outer surface of the chip.

The second type of on-chip test device was the Interdigitated Electrode Array (IDEA). An example IDE testing the Metal 1 layer is shown in Figure 5. Because of the relatively small features and large test area, there are about 10^{-4}squares (□) for leakage current to flow. If the ultimate sensitivity of the measurement was be approximately $5x10^{-16}$amperes for a 5 volt bias, the effective surface resistivity that can be sensed would be approximately $10^{-20}\Omega/\square$ which should provide early indication of potential faults with MOS circuit protection in biological systems.

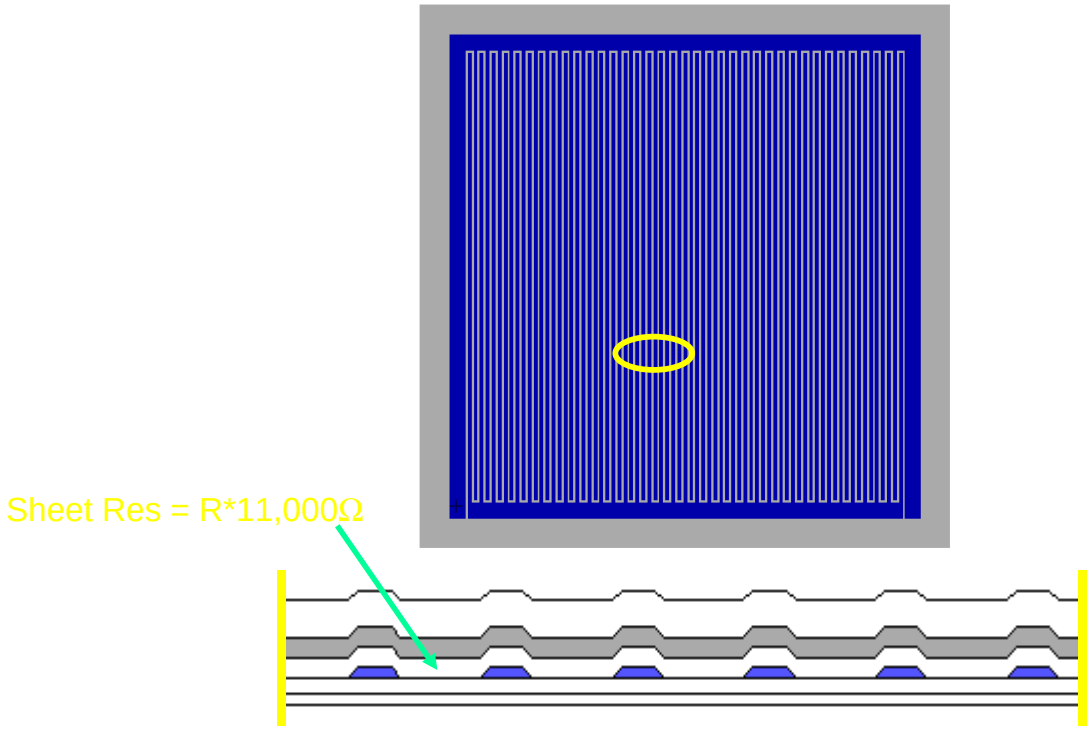


Figure 5: Interdigitated electrode array (IDEA) for MOSIS 2μm n-well process. IDEA is formed with Metal 1 while Metal 2 and the outer passivation layer provides additional protection.

SUMMARY OF PASSCHIP:

- Vertical Grids Check Dielectric Conductivity

- Interdigitated Electrode Arrays for Lateral Resistivity
- MOS Threshold Monitors
- Power and Bias Monitors
- External Test Device Connections
- Implantable in CNS with Transcutaneous Transmitter
- Lithium TC Batteries Supply 4uA for >9years
- Ultra-low power encode/mux/transmit circuit (3uA)

Preliminary Results of First Working Passchip

A new version of the PassChip was recently tested and found to be functional. This implementation utilized better models during the design of the integrator reset circuitry, and apparently had no lethal layout errors. The new version also incorporated an on-chip current reference for the circuit to eliminate the need for an external bias current. The 16 channel decoder was not yet ready for use when the chip was evaluated, but the scope photo in Figure 6 shows the output pulse interval train from the LED. Note the wide marker channel and the relative differences between data intervals corresponding to differences in the status of the output integrators for each channel.

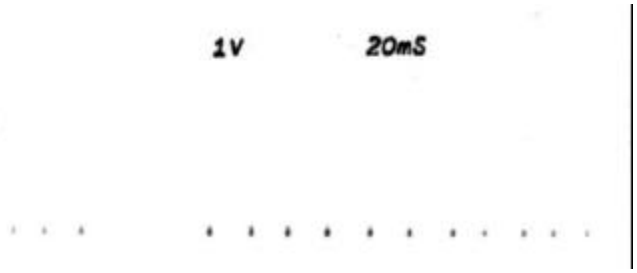


Figure 6: Oscilloscope photo of LED pulse train from 14 channel PassChip operating on 2.2μA of current from a 5 volt supply. Note channels 13 and 14 intervals before the marker channel with wide interval.

Figure 7 shows an oscilloscope photo of the output of a test version of the PassChip with extra connections for diagnostics. There were 6 channels in this PassChip with the output of one of the integrators pinned out for direct monitoring. Figure 7 lower trace shows the signal LED pulses marking the end of one output pulse interval and the beginning of the next. The top trace shows the output of the decoder integrator. At the end of each interval, the output voltage of the decoding integrator is proportional to the time of the interval. This output voltage will normally be acquired by the data acquisition system for conversion to leakage current.

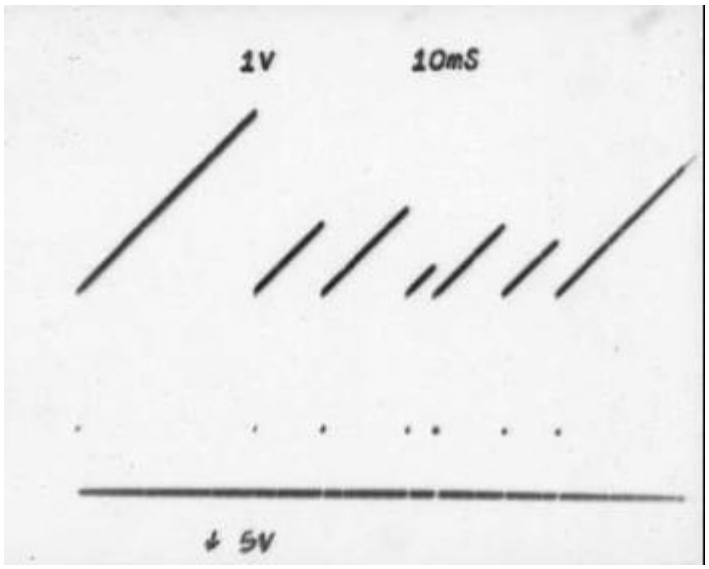


Figure 7: Oscilloscope photo of output of test PassChip which has a 6 channel multiplexed array of charge integrators for measuring femtoampere leakage currents. In the lower trace, the dots represent the LED output pulse which signals the beginning and end of a period for each channel. The upper trace is the output of a decoder integrator which produces a voltage at the end of a decoding integration period proportional to the pulse interval.

Figure 8 shows the output voltage directly measured from a test pin on the test PassChip. This particular device also had the charge integration node pinned out for testing. This is what the data file for each channel would look like except the slopes of the lines would be different for different leakage currents. The stairstep appearance is due to the sample and hold used to extract this data from the multiplexed waveform. The actual integration current was 1pA flowing onto an integration node capacitance of approximately 2pF. The resulting -0.5V/sec is just what we expect to observe since the integrator span on chip is 1 volt.

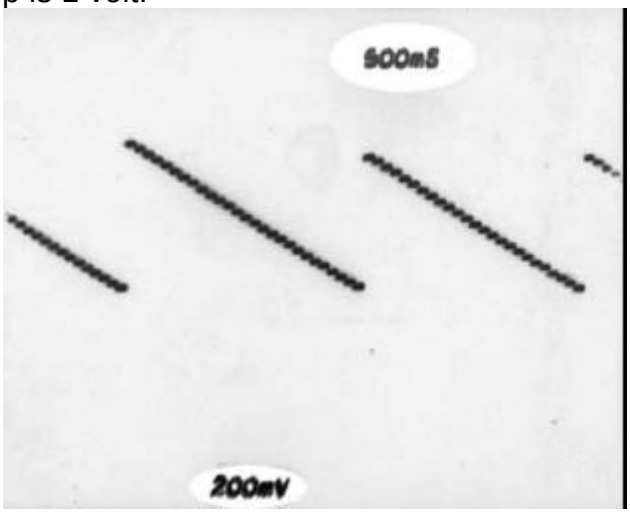


Figure 8: Oscilloscope photo of test PassChip Channel 4 integrator output. Slope of integrator output corresponds to a leakage rate of -0.5v/sec.

Other simple tests have further verified the design. For example, using the test PassChip, we open circuited the bias line and open circuited the sense line for the device that was pinned out. As expected, the integrator reset circuit was rendered inoperative causing the integrator output voltage to fall below the normal lower limit. In this way then the continuity of the test devices can be detected.

We have just begun characterizing this circuit, and will implement saline soak testing in May, 1999. Following this, if warranted, successful saline tested devices will be implanted in June of 1999.

Using a similar approach, a multichannel electrometer for evaluation of externally mounted test devices will be designed for the proposed study as outlined in Methods. For this device, most of the CMOS testers would be replaced with sets of bonding pads.